UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,630	09/20/2001	John Erik Lindholm	NVIDP055/P000369	4492

28875 7590 05/20/2004

SILICON VALLEY INTELLECTUAL PROPERTY GROUP
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER	
CHAUHAN, ULKA J	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,630	LINDHOLM ET AL.	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 26-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *53* is/are allowed.

6)☒ Claim(s) *1-10,12-24,26-52,54 and 55* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 25 is cancelled; claims 54 and 55 are newly added; claims 1-24 and 26-55 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 22-52 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification on pg. 68 discloses, "As mentioned earlier, the processing may include calculating a Taylor Series. To accomplish this calculation, information is looked up in a plurality of tables in operation 806 corresponding to the most significant bits extracted in operation 802, as processed by 804 Such retrieved information may include a first *n* (n=0, 1, 2) derivatives corresponding to the most significant bits. As an operation, the look-up operation may be based at least in part on the least significant bits in order to locate a closes table entry. In the alternative, larger tables may be utilized." The disclosure does not enabling for the limitation "a function in which an initial n derivatives are tabulated and accessed via an interpolation operation" as recited in independent claims 22, 31-34, and 51-52.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-10, 13-20, 54, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,689,695 to Read and U.S. Patent No. 6,298,438 to Thayer et al.

7. As per claims 1, 54, and 55, Read teaches an image data processing system including a multiprocessor integrated circuit constructed for image and graphics processing comprising plural digital image/graphics processors 71-74 [c. 10 ll. 49-c. 11 ll. 7]. Read discloses that each image/graphics processor includes data unit 110 for performing logical and arithmetic data operations, address unit 120, and program flow control unit 130 that operate simultaneously on different instructions in an instruction pipeline ("***performing programmable operations***") [c. 12 ll. 52-62 and c. 14 ll. 30-36]. Digital image/graphics processor 71 includes a local port data bus Lbus 103, global port source data bus Gsrc 105 and global port destination data bus Gdst 107 ("***receiving data***" and "***storing the output in memory***") [c. 15 ll. 62-c. 16 ll. 3]. Read discloses a

programmer utilizing the instruction set of the digital image/graphics processors ("***user utilizing instructions from a predetermined instruction set***") [c. 67 ll. 1-20] and performing conditional branch instructions ("***branching between the programmable operations***") [Fig. 38]. Read does not expressly teach and "***wherein a swizzle operation is performed for component remapping***". Thayer teaches a multi-media extension unit, MEU 90, that functions similar to a coprocessor floating-point unit having unique multimedia operations [c. 12 ll. 16-18]. The MEU includes an operand routing unit, ORU 124, for re-aligning operands within one source register prior to entering them into ALU 116 [c. 13 ll. 25-26] by swizzling bits within registers such that operands are shuffled as needed by an algorithm ("***wherein a swizzle operation is performed for component remapping***") [c. 17 ll. 45-53]. And Thayer discloses that an instruction encodes the ORU routing settings for each of slots ("***indicating a manner in which a plurality of source vector components are re-mapped***") [c. 18 ll. 38-44]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the ORU as taught by Thayer in combination with Read's digital image/graphics processors in order to align multiple operands in response to specific instructions thereby enhancing the throughput of many imaging algorithms.

8. As per claims 2-6, Read discloses programmable operations are branched to labels, wherein the labels are stored in a table and the programmable operations are branched to indexes in the table, each index is stored in an address register, and each index is calculated [c. 145 ll. 11, table 58, c. 143 ll. 25-35, c. 142 ll. 66-c. 143 ll. 20, and c. 143 ll. 48].

9. As per claim 7, Read discloses terminating the programmable operations after a predetermined number of operations have been performed [c. 162 ll. 16 and c. 166 ll. 56-62].

10. As per claims 8-10, Read discloses that the programmable operations are branched on condition codes, wherein the condition codes are sourced as EQ, NE, LT, GE, LE, GT, FL, TR [c. 115 ll. 26-60 and c. 117 ll. 59-61] and wherein the condition codes are maskable [c. 21 ll. 21-58 and table 17].

11. Claims 13-17, 19, 20 are similar in scope to claims 1-10, and are rejected under the same rationale.

12. As per claim 18, Read discloses that the write masks are controlled utilizing and AND operation [c. 5 ll. 40-44].

13. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,689,695 to Read and U.S. Patent No. 6,298,438 to Thayer et al and U.S. Patent No. 6,577,316 to Brethour et al, and U.S. Patent No. 6,163,837 to Chan et al.

14. As per claim 12, Read discloses some of the operations selected from the group consisting of a branch operation, call operation, a return operation, a cosine operation, a sine operation, a floor operation, a fraction operation, a set-on-equal-to operation, a set false operation, a set-on-greater-than, a set-on-less-than-or-equal operation, a set-on-not-equal-to operation, a set true operation, a no operation, address register load, move, multiply, addition, multiply and addition, reciprocal, reciprocal square root, three component dot product, four component dot product, distance vector, minimum, maximum, set on less that, set on greater or equal than, exponential base two, logarithm base two, exponential, logarithm, and/or light coefficients [c. 15 ll. 25-60, c. 18 ll. 55-c. 19 ll. 10, c. 115 ll. 26-67, c. 21 ll. 21-58, c. 94 ll. 19-38, c. 152 ll. 51, c. 146 ll. 3, c. 90 ll. 18, c. 62 ll. 7-9, c. 89 ll. 14-40]. Brethour discloses ALU module 22 for performing add, min, max operations [c. 7 ll. 40-43]; MAC 25 for performing

multiply and addition operations [c. 7 ll. 50-63]; reciprocal module 24 for performing reciprocal of floating point number; transcendental module 26 for performing exponential base 2, logarithm base 2, and inverse square root operations [c. 8 ll. 11-19]. Chan discloses the following instructions move, add, multiply, multiply and add, compare equal, compare less than or equal, minimum, maximum, exponentiation, reciprocal square root, pack, pixel distance, dot product [c. 11-c. 15]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined operations taught by Brethour and Chan with Read, in order to augment Read's instruction set and enhance the processing performed by the digital image/graphics processors.

15. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,689,695 to Read and U.S. Patent No. 6,577,316 to Brethour et al, and U.S. Patent No. 6,163,837 to Chan et al.

16. As per claim 21, As per claim 1, Read teaches an image data processing system including a multiprocessor integrated circuit constructed for image and graphics processing comprising plural digital image/graphics processors 71-74 [c. 10 ll. 49-c. 11 ll. 7]. Read discloses that each image/graphics processor includes data unit 110 for performing logical and arithmetic data operations, address unit 120, and program flow control unit 130 that operate simultaneously on different instructions in an instruction pipeline [c. 12 ll. 52-62 and c. 14 ll. 30-36]. Digital image/graphics processor 71 includes a local port data bus Lbus 103, global port source data bus Gsrc 105 and global port destination data bus Gdst 107 [c. 15 ll. 62-c. 16 ll. 3]. Read discloses a programmer utilizing the instruction set of the digital image/graphics processors [c. 67 ll. 1-20] and performing conditional branch instructions [Fig. 38] as well as some of the operations

selected from the group consisting of a branch operation, call operation, a return operation, a cosine operation, a sine operation, a floor operation, a fraction operation, a set-on-equal-to operation, a set false operation, a set-on-greater-than, a set-on-less-than-or-equal operation, a set-on-not-equal-to operation, a set true operation, a no operation, address register load, move, multiply, addition, multiply and addition, reciprocal, reciprocal square root, three component dot product, four component dot product, distance vector, minimum, maximum, set on less that, set on greater or equal than, exponential base two, logarithm base two, exponential, logarithm, and/or light coefficients [c. 15 ll. 25-60, c. 18 ll. 55-c. 19 ll. 10, c. 115 ll. 26-67, c. 21 ll. 21-58, c. 94 ll. 19-38, c. 152 ll. 51, c. 146 ll. 3, c. 90 ll. 18, c. 62 ll. 7-9, c. 89 ll. 14-40]. Brethour discloses ALU module 22 for performing add, min, max operations [c. 7 ll. 40-43]; MAC 25 for performing multiply and addition operations [c. 7 ll. 50-63]; reciprocal module 24 for performing reciprocal of floating point number; transcendental module 26 for performing exponential base 2, logarithm base 2, and inverse square root operations [c. 8 ll. 11-19]. Chan discloses the following instructions move, add, multiply, multiply and add, compare equal, compare less than or equal, minimum, maximum, exponentiation, reciprocal square root, pack, pixel distance, dot product [c. 11-c. 15]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined operations taught by Brethour and Chan with Read, in order to augment Read's instruction set and enhance the processing performed by the digital image/graphics processors.

17. Claims 22-24, 26, 27, and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,689,695 to Read and U.S. Patent No. 6,581,085 to Yue et al.

18. As per claims 22 and 27, Read teaches an image data processing system including a multiprocessor integrated circuit constructed for image and graphics processing comprising plural digital image/graphics processors 71-74 [c. 10 ll. 49-c. 11 ll. 7]. Read discloses that each image/graphics processor includes data unit 110 for performing logical and arithmetic data operations, address unit 120, and program flow control unit 130 that operate simultaneously on different instructions in an instruction pipeline [c. 12 ll. 52-62 and c. 14 ll. 30-36]. Digital image/graphics processor 71 includes a local port data bus Lbus 103, global port source data bus Gsrc 105 and global port destination data bus Gdst 107 [c. 15 ll. 62-c. 16 ll. 3]. Read discloses a programmer utilizing the instruction set of the digital image/graphics processors [c. 67 ll. 1-20]. Read does not expressly teach "***a function in which an initial n derivatives are tabulated and accessed via an interpolation operation***". Yue teaches an approximation circuit to approximate a function f(x), given an input value "x", by computing and adding at least the first two terms in a Taylor series (i.e., f(a) and f'(a)(x-a)) where "a" is an approximation that share the most significant bits of input value "x" [c. 1 ll. 20-26]. The values f(a), f'(a), and f"(a) are provided by look-up tables; a first look-up table receives the approximation value "a", and provides a function f(a), a second look-up table provides a first derivative f'(a), and a third look-up table provides a value of one half of the second derivative (1/2)f"(a) of the function f(a) [c. 1 ll. 26-42]. And Yue discloses that the approximation circuit is fast because look up tables take little time to generate bits representing f(a), f'(a), and (½)f"(a) [c. 4 ll. 8-10]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the approximation circuit as taught by Yue in combination with Read's digital image/graphics processor such that

the image/graphics processors is enhanced by being able to quickly generate functions based on the functions' Taylor series expansions.

19. As per claims 23 and 24, Read does not expressly teach trigonometric and hyperbolic functions. However, as sine, cosine, tangent, arctangent, exponential, logarithm, hyperbolic sine, hyperbolic cosine, hyperbolic tangent functions can be expressed by the Taylor series expansions, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the approximation circuit taught by Yue to implement the trigonometric and hyperbolic functions in combination with Read's digital image/graphics processor such that the image/graphics processors is enhanced by being able to quickly generate trigonometric and hyperbolic functions based the Taylor series expansions.

20. As per claim 26, Yue discloses floating point format [c. 2 ll. 33-39].

21. As per claim 30, Yue discloses that the terms in the Taylor series are computed in parallel [c. 1 ll. 46-47].

22. Claims 31, 32, and 33 are similar in scope to claim 22 and are rejected under the same rationale.

23. Claims 28 and 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,689,695 to Read and U.S. Patent No. 6,581,085 to Yue et al and U.S. Patent No. 6,385,632 to Choe et al.

24. As per claims 28 and 29, Read does not expressly teach the CORDIC algorithm or converting coordinate systems. Choe discloses that the CORDIC algorithm in its various realizations may be used to compute a variety of elementary functions such as, e.g., sine, cosine, tangent, arctangent, exponential, logarithm, hyperbolic sine, hyperbolic cosine, hyperbolic

tangent, etc. as well as two-dimensional rotations, multiplications, divisions and square roots [c. 1 ll. 16-22]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the CORDIC algorithm to compute certain trigonometric and hyperbolic functions as well as rotations, as taught by Choe in combination with Read's digital image/graphics processor such that the image/graphics processors is enhanced by being able to quickly generate functions based on the functions' Taylor series expansions.

25. Claims 34 and 37-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,689,695 to Read and U.S. Patent No. 6,597,363 to Duluk, Jr. and U.S. Patent No. 6,581,085 to Yue et al.

26. As per claims 34 and 41-48, Read teaches an image data processing system including a multiprocessor integrated circuit constructed for image and graphics processing comprising plural digital image/graphics processors 71-74 [c. 10 ll. 49-c. 11 ll. 7]. Read discloses that each image/graphics processor includes a data unit 110 for performing logical and arithmetic data operations, address unit 120, and program flow control unit 130, that operate simultaneously on different instructions in an instruction pipeline [c. 12 ll. 52-62 and c. 14 ll. 30-36]. Digital image/graphics processor 71 includes a local port data bus Lbus 103, global port source data bus Gsrc 105 and global port destination data bus Gdst 107 [c. 15 ll. 62-c. 16 ll. 3]. Read discloses a programmer utilizing the instruction set of the digital image/graphics processors [c. 67 ll. 1-20]. Read does not expressly teach "***pre-processing the input data based on the function to be executed***" or "***a function in which an initial n derivatives are tabulated and accessed via an interpolation operation***". Duluk discloses a method for executing a function, identifying the function to be executed on the input data [c. 7-8]; preprocessing the input data based on the

function to be executed on the input data; processing the input data utilizing a plurality of operations independent of the function to be executed on the input data [c. 5-6]. Yue teaches an approximation circuit to approximate a function f(x), given an input value "x", by computing and adding at least the first two terms in a Taylor series (i.e., f(a) and f'(a)(x-a)) where "a" is an approximation that share the most significant bits of input value "x" [c. 1 ll. 20-26]. The values f(a), f'(a), and f''(a) are provided by look-up tables; a first look-up table receives the approximation value "a", and provides a function f(a), a second look-up table provides a first derivative f'(a), and a third look-up table provides a value of one half of the second derivative (1/2)f''(a) of the function f(a) [c. 1 ll. 26-42]. And Yue discloses that the approximation circuit is fast because look up tables take little time to generate bits representing f(a), f'(a), and (½)f''(a) [c. 4 ll. 8-10]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the approximation circuit as taught by Yue in combination with Duluk's disclosure of OpenGL and D3D APIs and Read's digital image/graphics processor such that the image/graphics processors is enhanced by incorporating functions and procedures afforded by such APIs as well as being able to quickly generate desired functions based on the functions' Taylor series expansions.

27. As per claim 37, Read discloses performing 1's complement operation on the input data if the function to be executed on the input data is at least one of sine or cosine [c. 61 ll. 21-22 and c. 146 ll. 3].

28. As per claim 38, Read discloses performing a barrel shift operation [c. 17 ll. 58-c. 18 ll. 4].

29. As per claim 39, Yue discloses extracting a set of most significant bits and a set of lest significant bits from a mantissa [c. 2 ll. 33-39].

30. As per claim 40, Yue discloses conditionally adding a one (1) to the most significant bits [c. 3 ll. 53-61].

31. As per claim 49, Yue discloses that the terms in the Taylor series are computed in parallel [c. 1 ll. 46-50].

32. As per claim 50, Read discloses cosine function [c. 146 ll. 2-3].

33. Claims 51 and 52 are similar in scope to claim 34 and are rejected under the same rationale.

Allowable Subject Matter

34. Claim 53 is allowed.

35. Claims 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6288723 U.S. Patent No. 6128638 U.S. Patent No. 5764228 Baldwin

U.S. Patent No. 4905177

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Ulka Chauhan** whose telephone number is **(703) 305-9651**. The examiner can normally be reached Mon.-Fri. from 9:00 am to 4:00 pm. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

38. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-4700.

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
May 17, 2004